

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

S.O.I.TEC SILICON ON INSULATOR)
TECHNOLOGIES S.A. and SOITEC USA,)
Inc.,) JURY TRIAL DEMANDED
)
Plaintiffs,) Case No. 1:05-cv-00806-***
)
v.)
)
MEMC ELECTRONIC MATERIALS, INC.,)
)
Defendant.)

AMENDED NOTICE OF DEPOSITION

TO:

BY E-MAIL AND U.S. MAIL

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BY HAND

Patricia Smink Rogowski
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CONNOLLY BOVE LODGE & HUTZ LLP
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TAKE NOTICE that, pursuant to Federal Rule of Civil Procedure 30(b)(6), plaintiffs S.O.I.TEC SILCON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, Inc. ("Soitec") will take the depositions of one or more corporate representatives of defendant MEMC Electronic Materials, Inc., ("MEMC"), and the law firm of Senniger Powers by oral examination with respect to the topics listed on Exhibits A and B at the times and on the dates indicated on Exhibit C. Please take further notice that, pursuant to Federal Rule of Civil Procedure 30, Soitec will take the deposition of Robert Falster, in his individual capacity, at the times and on the dates indicated on Exhibit C.

All depositions will take place at the offices of Senniger Powers, One Metropolitan Square, Suite 1600, Saint Louis, MO 63102 and will continue from day to day, Saturdays, Sundays and holidays excluded, until completed. All depositions will be recorded by a certified stenographic court reporter authorized to administer oaths. All depositions will also be videotaped.

EDWARDS ANGELL PALMER & DODGE, LLP

/s/ Denise Seastone Kraft

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October 19, 2007

EXHIBIT A

30(b)(6) topics to MEMC

1. The development, process for manufacturing, and characterization of any low or no defect silicon wafers or device layers by MEMC Electronic Materials, Inc. ("MEMC"), including the silicon wafers referred to by MEMC as Perfect Silicon, High Performance Silicon, Semi Perfect Silicon, epitaxial silicon, annealed silicon, Advanta, Optia, or Aegis.
2. The development, process for manufacturing, and characterization of any silicon on insulator devices invented, made, sold, or marketed by MEMC.
3. The development, process for manufacturing, and characterization of silicon wafers with a region referred to by MEMC as a Magic Denuded Zone.
4. The development, process for manufacturing, and characterization of any silicon on insulator wafer comprising a device layer of material referred to by MEMC as Perfect Silicon, High Performance Silicon, Semi Perfect Silicon, epitaxial silicon, annealed silicon, Advanta, Optia, or Aegis and a handle layer that has a Magic Denuded Zone.
5. The development by MEMC of silicon wafers 300mm or more in diameter, including without limitation the development of silicon wafers 300mm or more in diameter that have "a central axis, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region, in which there is a predominant intrinsic point defect, which is substantially free of agglomerated intrinsic point defects."
6. The prosecution of United States Provisional Patent Application Serial No. 60/098,902 and the prosecution of any US or foreign patent application relating to the same subject matter as the '902 application or claiming priority to the '902 application, including without limitation, United States Patent Application Serial No. 09/387,288, which issued as United States Patent No. 6,236,104. (Collectively, the "SOI Applications".)
7. The prosecution of United States Provisional Patent Application Serial No. 60/041,845 and the prosecution of any US or foreign patent application relating to the same subject matter as the '845 application or claiming priority to the '845 application, including without limitation, United States Patent Application Serial No. 09/057,851, which issued as United States Patent No. 5,919,302. (Collectively, the "Bulk Silicon Applications".)
8. The conception of any invention claimed in any patent issuing from the SOI or Bulk Silicon Applications.
9. The reduction to practice of any invention claimed in any patent issuing from the SOI or Bulk Silicon Applications.

10. Any actual or indirect infringement, either literal or under the doctrine of equivalents, by S.O.I.TEC SILCON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, Inc. ("Soitec") of any claim of United States Patent No. 6,236,104.
11. Any allegations that any claim of United States Patent No. 6,236,104 is invalid.
12. Any allegations that any claim of United States Patent No. 6,236,104 is unenforceable.
13. Any opinion of counsel that any valid and enforceable claim of United States Patent No. 6,236,104 is infringed by declaratory judgment plaintiff Soitec.
14. MEMC's relationship with Soitec.
15. MEMC'S relationship with SiBond.
16. MEMC'S relationship with Ibis.
17. MEMC'S relationship with Silicon Genesis Corporation.
18. MEMC'S relationship with Professor Jae-gun Park or Hanyang University regarding silicon on insulator.
19. MEMC'S relationship with any person not a party to this lawsuit, including Samsung, regarding the investigation, development, manufacture, supply, sale, or marketing of silicon on insulator.
20. The testing of silicon wafers to determine the presence, type, amount and distribution of agglomerated intrinsic point defects.
21. The testing of silicon wafers to determine the presence, type, amount, and distribution of non-agglomerated intrinsic point defects.
22. MEMC'S licensing and efforts to license any patent relating to silicon wafers, silicon processing or the making of silicon on insulator, including without limitation any licensing of any patent issuing from any of the SOI or Bulk Silicon Applications.
23. Any covenant not to sue granted by MEMC to anyone relating to any patent issuing from any of the SOI or Bulk Silicon Applications.

EXHIBIT B

30(b)(6) topics to Senniger Powers:

1. The prosecution of United States Provisional Patent Application Serial No. 60/098,902 and the prosecution of any US or foreign patent application relating to the same subject matter as the '902 application or claiming priority to the '902 application, including without limitation, United States Patent Application Serial No. 09/387,288, which issued as United States Patent No. 6,236,104. (Collectively, the "SOI Applications".)
2. The preparation of the SOI Applications
3. The decision to name Robert Falster as the sole inventor on the SOI Applications.
4. The prosecution of United States Provisional Patent Application Serial No. 60/041,845 and the prosecution of any US or foreign patent application relating to the same subject matter as the '845 application or claiming priority to the '845 application, including without limitation, United States Patent Application Serial No. 09/057,851, which issued as United States Patent No. 5,919,302. (Collectively, the "Bulk Silicon Applications".)
5. Senniger Powers' procedures, in existence from September 2, 1998, until May 22, 2001, for complying with any duty of disclosure, including without limitation the disclosure of references, to the United States Patent and Trademark Office ("USPTO") in connection with the prosecution of patent applications pending before that agency.
6. The contribution of Robert A. Falster to each invention claimed in United States Patent No. 6,236,104.
7. The contribution of each named inventor to each invention claimed in United States Patent No. 5,919,302.

EXHIBIT C

Date	Designee	Topic(s)
October 22, 2007	Joseph Holzer	Exh. A: 1, 5
October 23, 2007	Edward Hejlek	Exh. A: 6, 7, 11-12
October 25, 2007	Shaker Sadasivam	Exh. A: 14-19, 22, 23; Exh. B
To be determined	Robert Falster	Exh. A: 2, 3, 20, 21
To be determined	Robert Falster (and in his individual capacity)	Exh. A: 4, 8, 9
To be determined	Expert witness	Exh. A: 20
To be determined	Expert witness	Exh. A: 21
To be determined	To be determined	Exh. A: 10

CERTIFICATE OF SERVICE

I hereby certify that on this 19th day of October, 2007, a true and correct copy of the foregoing was electronically filed with the Clerk of the Court using the CM/ECF system and a copy was served upon the following counsel of record in the manner indicated:

BY E-MAIL AND U.S. MAIL

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